SONY

A Challenge for 3 µm SPAD Pixel Using Embedded Metal Contact on Deep Trench Pixel Isolation

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Outline

- 1. Overview of Sony's SPAD technology
- 2. A Challenge for shrinking the pixel size
- 3. Prototyping
- 4. Conclusions

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Overview of Sony's SPAD technology



- Down to 6 µm pixel technology with relatively large PDE
- SPAD sensors combining the pixel and advanced circuit design.

Pixel technology



[4] K. Ito *et al*., IEDM 2020

[1] S. Shimada *et al.*, IEDM 2021

- High fill-factor owing to the back-illuminated stacked structure.
- High PDE without timing jitter degradation by optimizing the potential slope

Pixel technology



^[1] S. Shimada *et al.*, IEDM 2021

- PDE is above 20 % at 940 nm of wavelength
- Timing jitter is less than 150 psec of FWHM

LiDAR system



- A SPAD Direct Time-of-Flight Depth Sensor has been developed for automotive LiDAR applications
- High-sensitivity depth sensors make it possible to measure long distances

LiDAR system



[5] O. Kumagai et al., ISSCC2021

 The LiDAR is capable of detecting objects 150m ahead at day light with poor object detection ratio, even if the reflectance is less than 10%

Photon counting image sensor



• SPAD Photon counting Image sensor created by introducing extrapolating photon count to reduce in-pixel counter bit and power consumption in a pixel

HDR image capture



HDR image capture at 250 fps



[2] J.Ogi *et al.,* ISSCC 2021 [3] J.Ogi *et al.,* ISSW 2021

• 250 fps and 124 dB HDR was achieved only with the 9-bit in-pixel counter

Outline

1. Overview of Sony's SPAD technology

2. A Challenge for shrinking the pixel size

- 1. Motivation
- 2. Pixel structure
- 3. Potential design
- 3. Prototyping

4. Conclusions

A challenge for shrinking the pixel size



• We challenge to shrink the SPAD pixel size to 3 µm by introducing a new SPAD pixel structure - Embedded metal contact on deep trench pixel isolation -

Motivation behind shrinking the pixel size



• A small pixel contributes to improve the SPAD sensor characteristics under high light illumination, such as, photon counting saturation.

Small pixel technology

N+
P+
STI
N-well
P-well
Metal



[6] K. Morimoto *et al* Optic Express Apr, 2020

[7] Z. You *et al.*,, ISSW2017

- Electric filed on the pixel edge must be decreased for a small pixel.
- The embedded metal contact is introduced with improved guard ring design



Embedded metal contact structure

- The metal contact is embedded in the two-step deep trench isolation
- The embedded metal contact separates the anode and cathode region in a vertical direction

Two-step full trench isolation structure



- The two-step trench isolation has an advantageous trench width for combining the embedded contact and optical shield for cross talk suppression.
- The embedded metal is also used as a low impedance metal wiring.

Improvement of avalanche region design



 Small and deep avalanche region reduces the electric field around the pixel surface and suppress edge breakdown.

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3. Prototyping

- 1. Chip design
- 2. Multiplication and dark count rate (DCR)
- 3. Photon detection efficiency (PDE)
- 4. Cross Talk (CT) Probability
- 5. Captured image with photon counting circuit

4. Conclusions

Prototyping for the proof of concept



pitch pixel front end circuit with 14-bit in-pixel counter.

circuit

Breakdown characteristics



- Breakdown operation with the 3.06-µm-pitch pixels is demonstrated.
- V_{bd} variation is less than 100 mV.

Improvement of the dark count rate



• DCR is successfully reduced with the optimized potential design to decrease the electric field around the pixel surface.

Photon detection efficiency



Measured at *Photon detection rate to incident photons on the whole pixel area (3.06 μ m \square)

• The photon detection efficiency is 57% even with the small pixel size because of the optimized potential slope for the electron transfer.

Cross-talk (CT) probability



The cross-talk probability is less than 0.4 % owing to the full trench isolation with the two-step full trench isolation.

Captured image with the 3 µm pixel array



- ✓ 160 x 264 pixels readout with on-chip color filter
- ✓ 1/60 sec exposure
- ✓ Room temperature
- The color image has been obtained with the 3.06 µm SPAD pixel array and photon counting circuit of the 14-bit pixel parallel counter

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PDE and DCR comparison



- PDE is significantly increased compared with the previous works for pixels smaller than or equal to 5 µm.
- DCR and PDE are comparable to those with 6 µm pixels.

Characteristics comparison

	Unit	[3]	[1]	[8]	[9]	[7]	[6]			This work
Pixel pitch	μm	6.12	6	6.39	5	3	4	3	2.2	3.06
Array size		160x 264	N/D	2072x 1548	N/D	4x4	4x4			160x264
Technology		BI-3D 90nm	BI-3D 90nm	BI-3D 90nm	FI	FI 130nm	Fl 180nm			BI-3D 90nm
V _{bd}	V	N/D	22	30	N/D	15.8	22.1	23.6	32.35	20.9
V _{ex}	V	3	3	2.5	5.8 ^{*2}	1.2	6	6	6	3
Peak PDE	%	58	66.7 ^{*1}	69.4	12 ^{*1*2}	6 ^{*2}	14.2	5.6	2	57
DCR@25° C	cps	35.4	19	1.8	17.3 ^{*2}	1343	2.5	1.6	751	15.8
Cross talk	%	N/D	* 0_N5 data	of the beak PD	E. the argest	val ceOn 2 ^{*3}	icl 3 s57ed.	2.75	2.97	<0.2

*2 No numerical value is expressed in the articles. Author calculated the value from the graphs in the articles.

- The 3 µm SPAD pixel has been demonstrated.
- We aim to improve the pixel characteristics further, in order to utilize such small pixel in a high-resolution photon counting image sensor.

Conclusions

- Sony has developed advanced SPAD sensors combining the relatively high-PDE pixels and advanced circuit designs.
- The SPAD pixel size is shrunk to 3 µm by introducing embedded metal contact on deep trench pixel isolation.
- The peak PDE using a green color filter is 57 % and cross talk probability is less than 0.4 %, while the DCR is 15.8 cps with 20.9 V of V_{bd} and 3 V of V_{ex}.
- DCR and PDE are comparable to those with 6 µm pixels. This is achieved with the embedded contact and optimized potential design for the multiplication.
- We are now trying to improve the pixel characteristics further.